IDEC Chip Design Contest

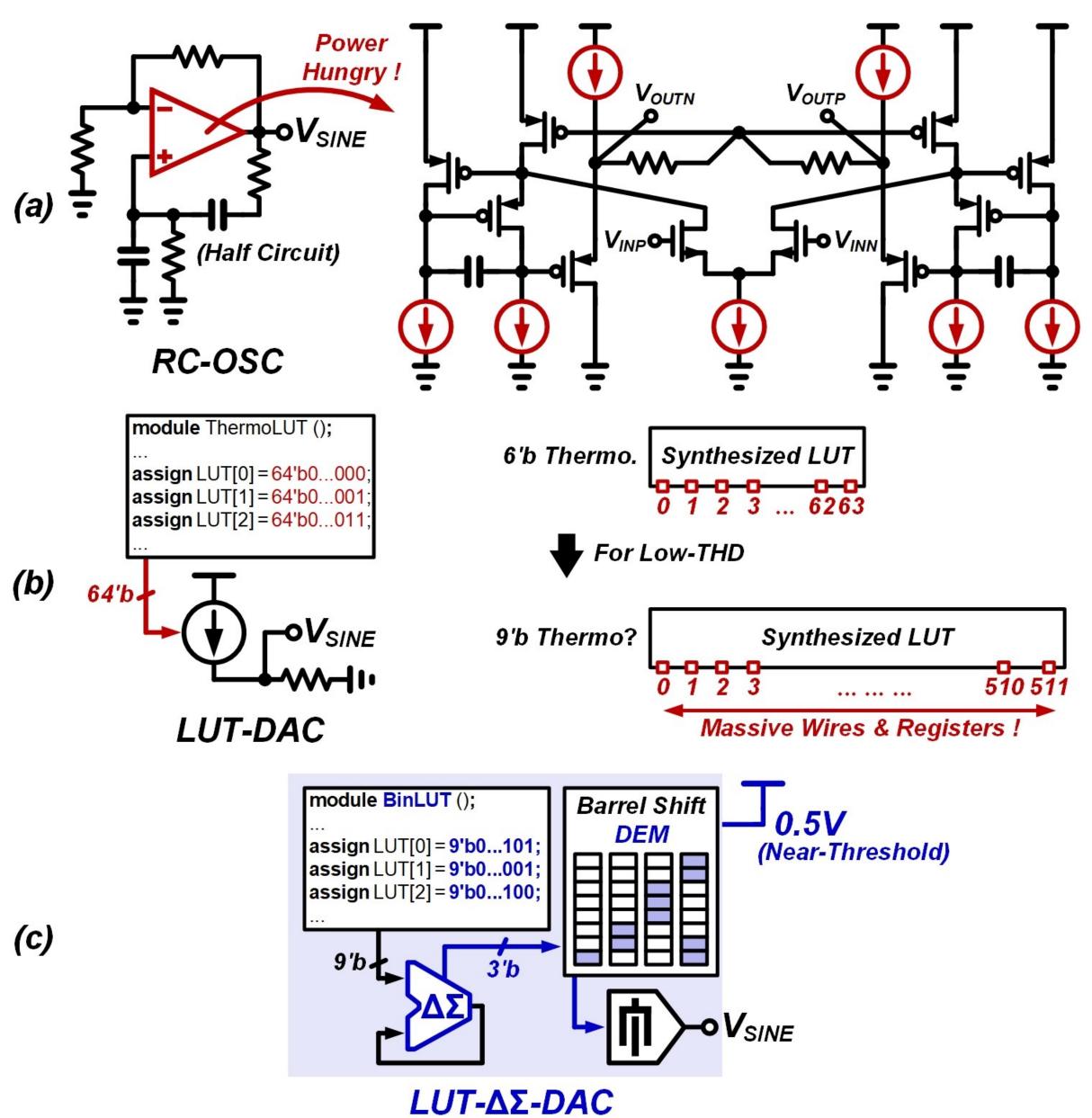


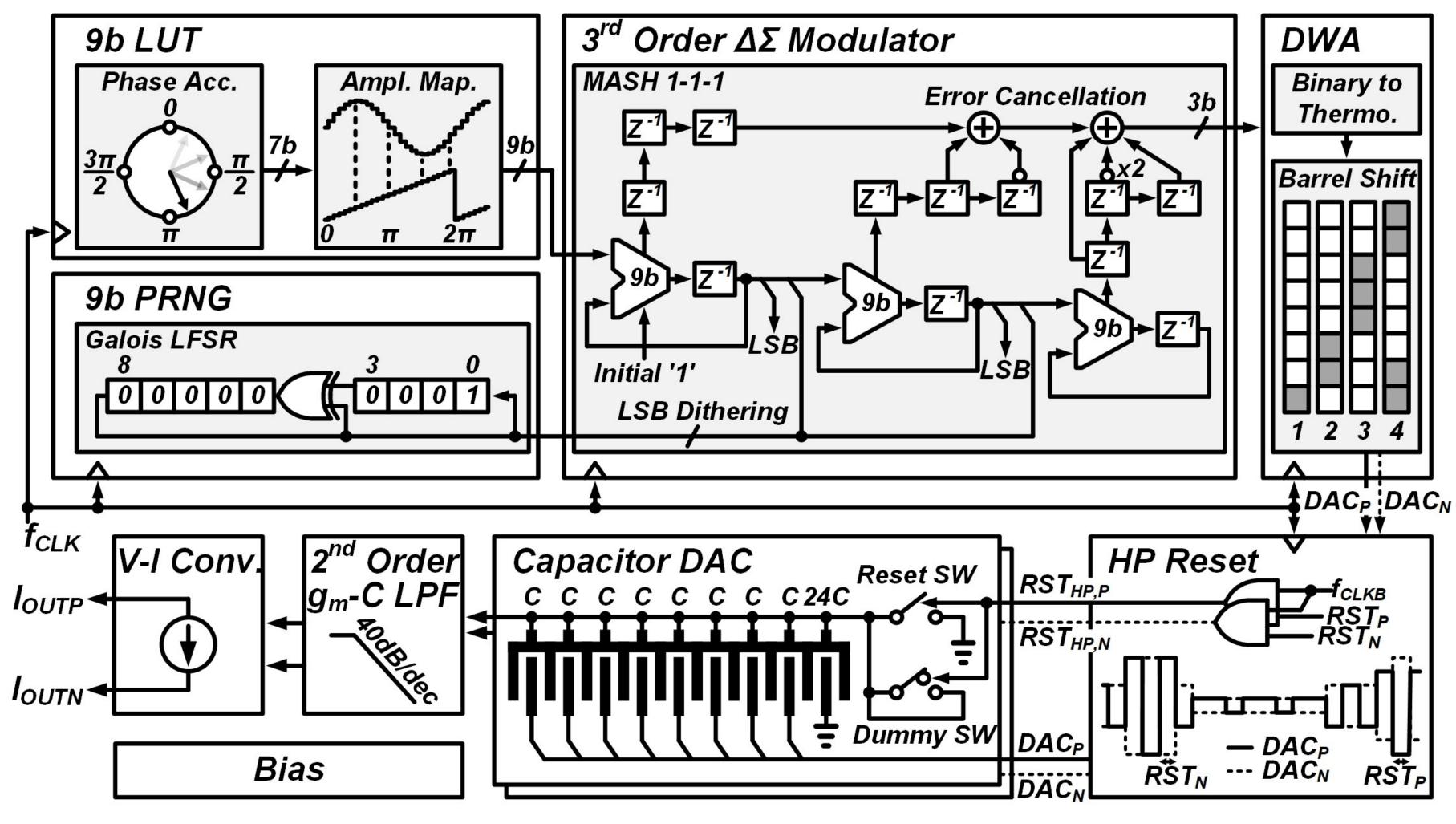
A 0.5V, 6.2μW, 0.059mm² Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing

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The First Sub-10µW, Sub-0.1% THD Sinusoidal CG IC for Bio-Z Sensing Applications

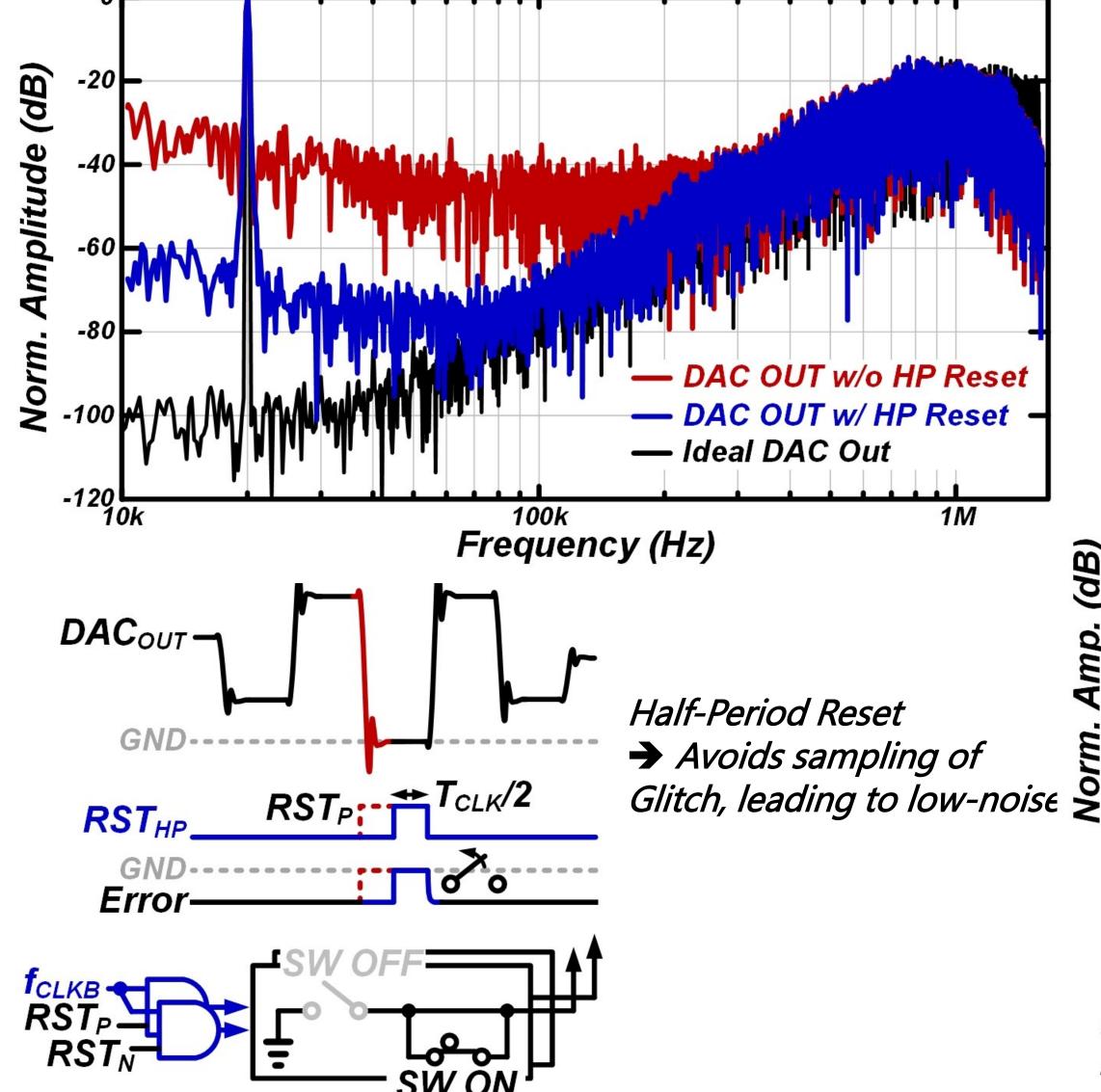




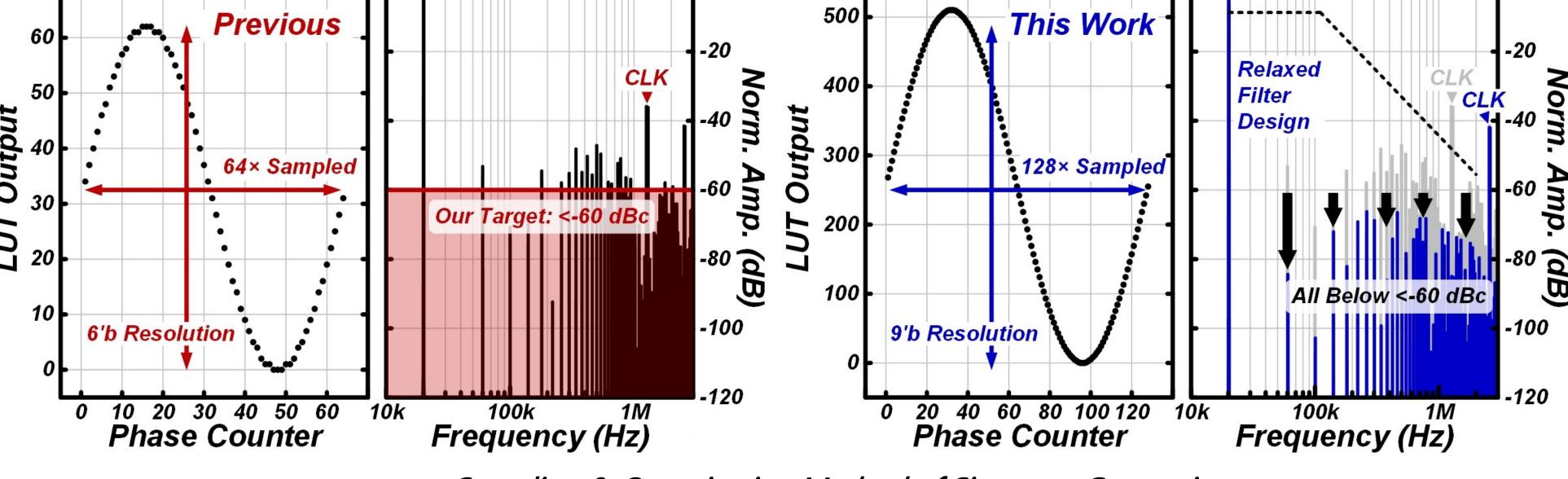
Overall Architecture of the Proposed Mixed-Signal Sinewave Generator

(a) RC-OSC → High-Power due to the analog OTA
(b) LUT-DAC → High-Power & Large-Area due to the increased routing wires & registers

(c) LUT-ΔΣ-DAC → Reduced wires & registers, thus low-power & small-area



This Work is Presented in VLSI Symposium 2020



Sampling & Quantization Method of Sinewave Generation

Oversampling & Fine Quantization → Reduced spur levels

0.5V Near-Threshold Operation → Low-power consumption

2. Retiming Logic

3. Capacitor DAC

6. Test Circuit

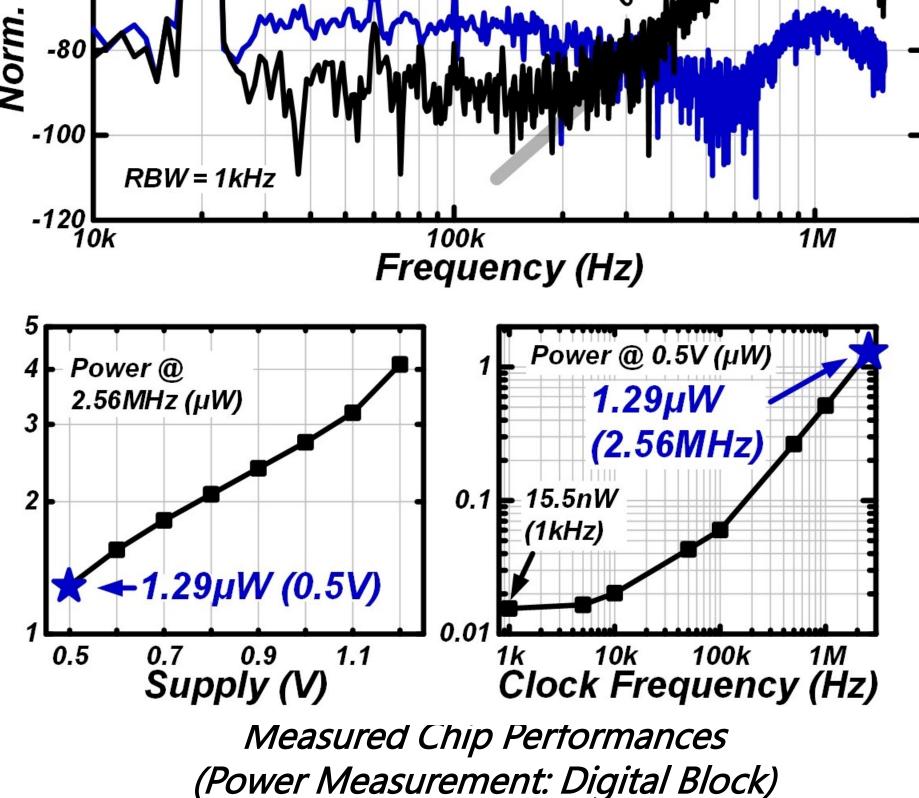
Elses: Decap

4. LPF

. LUT+PRNG+ΔΣMod.+DWA

5. V-I Converter

7. Bias



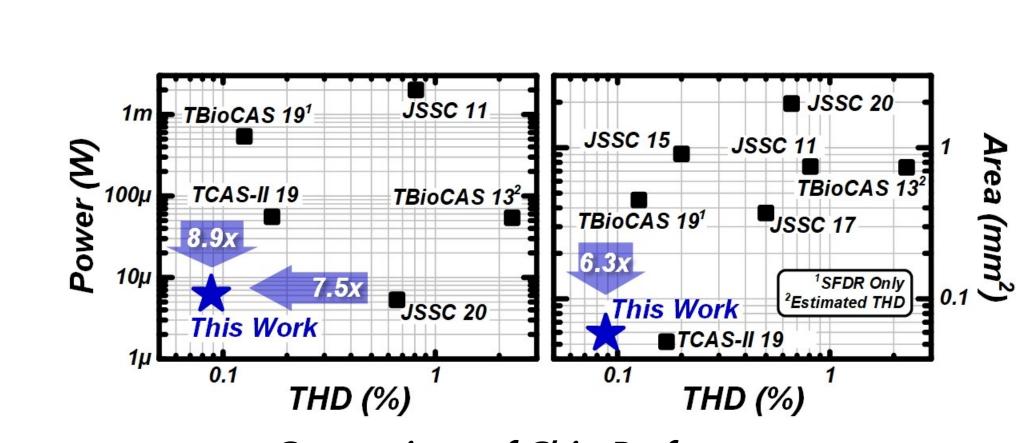
65.17dBc

-20

- CG Output (SFDR = 65.17dBc)

— DAC Output (SFDR = 73.8dBc)

THD = 0.088%



Chip Photograph

Synthesized

Digital Core

Comparison of Chip Performance